Amendments to the Claims:

1. (Cancelled)

25. (New) An enhanced VSB receiver for receiving and decoding an input signal including main data and enhanced data transmitted from a VSB transmitter, the enhanced VSB receiver comprising:

a symbol indicator for indicating whether each symbol included in the input signal corresponds to the main data or enhanced data;

a main VSB processor for processing the input signal received from the VSB transmitter in a reverse order of the VSB transmitter and outputting a multiplexed data signal;

a demultiplexer for demultiplexing the multiplexed data signal received from the main VSB processor into the main data and the enhanced data; and

a supplemental VSB processor for decoding the enhanced data demultiplexed from the demultiplexer to obtain original data.

26. (New) The enhanced VSB receiver of claim 25, wherein the main data included in the input signal comprises MPEG data.

27. (New) The enhanced VSB receiver of claim 25, wherein the symbol indicator comprises:

a multiplexer for receiving and multiplexing an enhanced data dummy packet and a main data dummy packet and outputting as a multiplexer output signal;

a randomizer for randomizing the multiplexer output signal;

a parity inserter for inserting dummy bytes to the randomized data;

a data interleaver for interleaving an output of the parity inserter; and

a trellis coder for converting the interleaved data to symbols and outputting the converted symbols without subjecting to trellis coding.

28. (New) The enhanced VSB receiver of claim 27, wherein the trellis coder comprises a plurality of coders and precoders for receiving the symbols and forwarding the symbols without subjecting to precoding and coding.

29. (New) The enhanced VSB receiver of claim 27, wherein each symbol outputted from the trellis coder includes two bits D1 and D0, wherein if the bit D1 is at a first logic level, a corresponding symbol included in the input signal corresponds to a enhanced data symbol, and if the bit D1 is at a second logic level, the symbol corresponds to a main data symbol.

30. (New) The enhanced VSB receiver of claim 29, wherein if the bit D1 is at the first logic level, the bit D0 represents one of a sequence of null bits included in the enhanced data.

31. (New) The enhanced VSB receiver of claim 27, wherein the randomizer subjects the multiplexer output signal using pseudo random bytes and 0x55 to a bit-wise AND logical operation, and a result of the AND logic operation and input bits from the multiplexer to a bit-wise exclusive OR logical operation.

32. (New) The enhanced VSB receiver of claim 27, wherein the main data dummy packet produces 187 dummy bytes of 0x00, and the enhanced data dummy packet produces 3 dummy bytes of 0x00 corresponding to header bytes, and 184 dummy bytes of 0xAA corresponding to the enhanced data.

33. (New) The enhanced VSB receiver of claim 25, wherein the symbol indicator generates a sequence of null bits included in the enhanced data.

34. (New) The enhanced VSB receiver of claim 33, wherein the main VSB processor comprises:

a demodulator for receiving the input signal, converting the input signal into a base band signal, and recovering a segment synchronizing signal, a field synchronizing signal, and a symbol timing from the base band signal;

a comb filter for removing an NTSC interference signal from an output signal of the demodulator, if the NTSC interference signal is detected;

a slicer predictor for providing a slicer prediction signal and a prediction reliability signal by using the sequence of null bits generated from the symbol indicator;

a channel equalizer for correcting a distorted channel in an output signal of the comb filter by using the slicer prediction signal, the prediction reliability signal, and the sequence of null bits and outputting a channel equalizer output signal;

a phase tracker for correcting a phase of the channel equalizer output signal by using the sequence of null bits and the slicer prediction signal;

a trellis decoder for decoding the phase-corrected signal using Viterbi algorithm and the sequence of null bits received from the symbol indicator;

a data deinterleaver for deinterleaving a trellis decoder output signal;

a Reed-Solomon decoder for decoding a Reed-Solomon coded signal outputted from the data deinterleaver; and

a data derandomizer for derandomizing a Reed-Solomon decoder output signal.

35. (New) The enhanced VSB receiver of claim 34, wherein the Reed-Solomon decoder of the main VSB processor removes 20 parity bytes without subjecting the enhanced data to Reed-Solomon decoding.

36. (New) The enhanced VSB receiver of claim 34, wherein the demultiplexer demultiplexes the multiplexed data signal from the main VSB processor into the main data and the enhanced data by using a multiplexing information signal detected from the field synchronizing signal.

37. (New) The enhanced VSB receiver of claim 25, wherein the supplemental VSB processor comprises:

a header remover for removing header bytes from the enhanced data received from the demultiplexer;

a null sequence remover for removing a sequence of null bits inserted to the enhanced data; and

a Reed-Solomon decoder for subjecting a null sequence remover output to Reed-Solomon decoding.

38. (New) The enhanced VSB receiver of claim 37, wherein the supplemental VSB processor further comprises a deinterleaver between the null sequence remover and the Reed-Solomon decoder for deinterleaving the null sequence remover output.

39. (New) The enhanced VSB receiver of claim 34, wherein the channel equalizer comprises:

a plurality of slicers, each slicer having a predetermined signal level detector;

a feed-forward filter for receiving a comb filter output signal;

a feedback filter for receiving an output signal of one of the plurality of slicers;

an adder for adding output signals of the feed-forward filter and the feedback filter and outputting an added signal as a channel equalizer output signal, wherein the plurality of slicers commonly receive the added signal;

a multiplexer for outputting one of the outputs of the plurality of slicers to the feedback filter in response to a control signal; and

a controller for updating filter coefficients of the feed-forward filter and the feedback filter and providing the control signal to the multiplexer in response to a multiplexer output signal, the slicer prediction signal, and the prediction reliability signal, the channel equalizer output signal, and the sequence of null bits to select the multiplexer to output signal from one of the plurality of slicers that has the predetermined signal level detector closes to the comb filter output signal.

40. (New) The enhanced VSB receiver of claim 39, wherein the slicer predictor receives the channel equalizer output signal, the sequence of null bits generated from the symbol indicator and information that the symbol received is of the enhanced data, estimates a register value of the trellis coder, calculates prediction reliability, and forwards the estimated register value to the controller of the channel equalizer.

41. (New) The enhanced VSB receiver of claim 40, wherein the plurality of slicers includes first to third slicers for processing main data symbols, and forth to nine slicers for processing the enhanced data symbols, wherein the first slicer has 8 level values of -7, -5, -3, -1, +1, +3, +5, +7, the second slicer has 4 level values of -7, -3, +1, +5, the third slicer has 4 level values of -5, -1, +3, +7, the fourth slicer has 4 level values of -7, -5, +1, +3, the fifth slicer has 4 level values of -3, -1, +5, +7, the sixth slicer has 2 level values of -7, +1, the seventh slicer has 2 level values of -5, +3, the eighth slicer has 2 level values of -3, +5, and the ninth slicer has 2 level values of -1, +7.

42. (New) The enhanced VSB receiver of claim 41, wherein with respect to the main data symbols, the first slicer is selected in a low reliability case, the second slicer is selected for a high reliability case the estimated register value is at a first logic level, and the third slicer is selected for a high reliability case and the estimated register value is at a second logic level.

43. (New) The enhanced VSB receiver of claim 41, wherein with respect to the enhanced data symbols;

one of the fourth slicer and the fifth slicer is selected in response to the null bit value for a low reliability case;

the sixth slicer is selected for a high reliability case and the null bit value and the estimated register value are at a first logic level;

the seventh slicer is selected for a high reliability case and the null bit value is at a first logic level and the estimated register value is at a second logic level;

the eighth slicer is selected for a high reliability case and the null bit value is a second logic level and the estimated register value is at a first logic level; and

the ninth slicer is selected for a high reliability case and the null bit value and the estimated register value are at a second logic level.

44. (New) The enhanced VSB receiver of claim 34, wherein the symbol indicator is responsive in synchronous to the field synchronizing signal.

45. (New) A method of receiving and decoding a terrestrial broadcasting signal transmitted from a VSB transmitter, the method comprising:

receiving an input signal from the VSB transmitter, the input signal including main data and enhanced data;

indicating whether each symbol included in the input signal corresponds to the main data or the enhanced data;

processing the input signal received from the VSB transmitter in a reverse order of the VSB transmitter and outputting a multiplexed data signal;

demultiplexing the multiplexed data signal into the main data and the enhanced data; and

decoding the demultiplexed enhanced data to obtain original data.

46. (New) The method of claim 45, wherein the indicating whether each symbol included in the input signal corresponds to the main data or the enhanced data comprises:

receiving and multiplexing an enhanced data dummy packet and a main data dummy packet and outputting as a multiplexed signal;

randomizing the multiplexed signal;

inserting dummy bytes to the randomized data;

interleaving the dummy-byte-inserted data; and

converting the interleaved data to symbols and outputting the converted symbols without subjecting to trellis coding.

47. (New) The method of claim 46, wherein each converted symbol includes two bits D1 and D0, wherein if the bit D1 is at a first logic level, a corresponding symbol included in the input signal corresponds to a enhanced data symbol, and if the bit D1 is at a second logic level, the symbol corresponds to a main data symbol.

48. (New) The method of claim 47, wherein if the bit D1 is at the first logic level, the bit D0 represents one of a sequence of null bits included in the enhanced data.

49. (New) The method of claim 47, wherein the indicating whether each symbol included in the input signal corresponds to the main data or the enhanced data comprises generating a sequence of null bits included in the enhanced data.

50. (New) The method of claim 49, wherein the processing the input signal received from the VSB transmitter comprises:

converting the input signal into a base band signal and recovering a segment synchronizing signal, a field synchronizing signal, and a symbol timing from the base band signal;

removing an NTSC interference signal from the converted base band signal, if the NTSC interference signal is detected;

generating a slicer prediction signal and a prediction reliability signal by using the sequence of null bits;

correcting a distorted channel in the interference-signal-removed signal by using the slicer prediction signal, the prediction reliability signal, and the sequence of null bits and outputting a channel-equalized signal;

correcting a phase of the channel-corrected signal by using the sequence of null bits and the slicer prediction signal;

trellis-decoding the phase-corrected signal using Viterbi algorithm and the sequence of null bits;

deinterleaving the trellis-decoded signal;

Reed-Solomon decoding the deinterleaved signal; and

derandomizing the Reed-Solomon-decoded signal.

51. (New) The method of claim 50, wherein the Reed-Solomon decoding the deinterleaved signal comprises removing 20 parity bytes from the deinterleaved signal without subjecting the enhanced data to Reed-Solomon decoding.

52. (New) The method of claim 50, wherein the demultiplexing the multiplexed data signal into the main data and the enhanced data comprises:

detecting a multiplexing information from the field synchronizing signal; and

demultiplexing the multiplexed data signal into the main data and the enhanced data using the detected multiplexing information.

53. (New) The method of claim 45, wherein the decoding the demultiplexed enhanced data to obtain original data comprises:

removing header bytes from the demultiplexed enhanced data;

removing a sequence of null bits included in the header-removed enhanced data; and

Reed-Solomon decoding the null-bit-removed data to obtain the original data.

54. (New) The method of claim 53, wherein the decoding the demultiplexed enhanced data to obtain original data further comprises deinterleaving the null-bit-removed data.